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<b>PRE-APPEAL BRIEF REQUEST FOR REVIEW</b>		Docket Number (Optional)	
		2003-0250 / 24061.144	
<p>I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]</p> <p>on <u>August 11, 2006</u></p> <p>Signature <u>Linda Ingram</u></p> <p>Typed or printed name <u>Linda Ingram</u></p>		Application Number	Filed
		10/754,178	January 9, 2004
		First Named Inventor	
		Ming Huan Tsai, et al.	
		Art Unit	Examiner
		2891	Bradley Smith

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

- applicant/inventor.
- assignee of record of the entire interest.  
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.  
(Form PTO/SB/96)
- attorney or agent of record.  
Registration number \_\_\_\_\_
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August 11, 2006

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.  
Submit multiple forms if more than one signature is required, see below\*.

<input checked="" type="checkbox"/>	*Total of <u>1</u> forms are submitted.
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This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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## REASONS

Claims 1-26 have been allowed, and are not part of the group of claims that has been appealed. The appeal is directed to the rejection of Claims 27-31, and the following discussion addresses Claims 27-31.

### Independent Claim 27

In the final rejection mailed on April 12, 2006, independent Claim 27 was rejected under 35 U.S.C. §102 as anticipated by Vahedi U.S. Patent Application Publication No. 2003/0148224. However, it is respectfully submitted that this §102 rejection is clearly not proper and is without basis. More specifically, as discussed below, this §102 rejection has a clear legal deficiency, because it lacks an essential element needed to establish a *prima facie* rejection.

Figure 1 of the present application depicts a substrate that includes a layer 30 of low-k dielectric. A layer of material 40 is provided on the dielectric layer 30, and the layer 40 is a bottom anti-reflective coating (BARC). A patterned photoresist layer 50 with openings 60 is disposed on the BARC layer 40. With reference to Figure 2, the BARC layer 40 is etched through the openings 60 in the photoresist layer 50. As discussed in Applicants' specification, the gas mixture used during this etching includes an etchant and a controller, and etches the BARC layer 40 while protecting the photoresist layer 50.

Figure 7 of the present application depicts another embodiment that includes a layer 30 of low-k dielectric. A layer of material 90 is provided on the dielectric layer 30, and the layer 90 is a BARC. A patterned photoresist layer 100 with an opening 102 is disposed on the BARC layer 90. With reference to Figure 8, the BARC layer 90 is etched through the opening 102 in the photoresist layer 100. As discussed in Applicants' specification, the gas mixture used during this etching includes an etchant and a controller, and etches the BARC layer 90 while protecting the photoresist layer 100. (Applicants wish to add that the foregoing discussion of some embodiments in Applicants' drawings is provided by way of example, and is not intended to imply any limitation to the scope of the pending claims).

Applicants turn now to the Vahedi reference. In explaining the rejection of Claim 27, the final rejection relies on paragraphs [0059] to [0068] of Vahedi. These paragraphs are discussing Figure 3A of Vahedi. Figure 3A shows a material layer 15 that is provided on a substrate 12.

(The substrate 12 is not visible in Figure 3A, but is visible in other figures, for example in Figure 4). Still referring to Figure 3A, a patterned photoresist 18a-18d is provided on the material layer 15, and the photoresist 18a-18d has openings through it. A polymer layer 24 is formed on the photoresist 18a-18d. Figure 3B shows an etching process 20-20' that etches the photoresist 18a-18d. As discussed in paragraph [0073], the process 20-20' not only etches the photoresist 18a-18d, but also etches away the polymer layer 24. Consequently, the polymer layer 24 provides some temporary protection for the photoresist 18a-18d during initial etching 20-20' of the photoresist (as discussed in paragraph [0063]), but the polymer layer 24 is also completely etched away during that same etching process (as discussed in paragraph [0073]). Consequently, it is relevant to note that the protection provided by the polymer layer 24 occurs only during etching of the photoresist 18a-18d, and not during later etching of the material layer 15.

More specifically, at the end of the etching process 20-20' in Figure 3B, the device appears as shown in Figure 3C, where the polymer layer 24 has been completely removed, but the material layer 15 has not yet been etched at all. Still referring to Figure 3C, a further etching process 32 is subsequently carried out, in order to etch the material layer 15. Figure 4 shows the device at the end of this second etching process 32. Since the polymer layer 24 was completely removed during the first etching process 20-20', and thus before the start of the second etching process 32, the polymer layer 24 is not present to protect the photoresist 18a-18d during the second etching process 32. In fact, contrary to the assertions in the final rejection, the photoresist 18a-18d is not protected at all from the etching process 32. As a result, the etching process 32 not only etches the material layer 15, but also etches the photoresist 18a-18d. In fact, the etching process 32 etches away almost all of the photoresist 18a-18d. This is readily evident by visually comparing Figure 3C (showing the photoresist 18a-18d at the start of the etching process 32) to Figure 4 (showing the photoresist 18a-18d at the end of the etching process 32).

Applicants' independent Claim 27 recites:

A method comprising:  
providing an integrated circuit device having a substrate  
and a material layer above the substrate;

forming a patterned photoresist layer including at least one opening therein above the material layer; and  
etching the material layer while protecting the photoresist layer from etching by exposing the integrated circuit device to a mixture including an etchant and a controller.

MPEP §2131 specifies that, in order for a reference to anticipate a claim under §102, the reference must teach each and every element recited in the claim, and must show these elements arranged in the same manner as recited in the claim. Vahedi does not meet this requirement. Contrary to the assertions in the final rejection, when Vahedi carries out his second etching step 32 in order to etch his material layer 15 (Figure 3C to Figure 4), his photoresist 18a-18d is not protected, and in fact virtually all of this photoresist is etched away. Vahedi thus does not disclose "etching the material layer while protecting the photoresist layer from etching", much less achieving this "by exposing the integrated circuit device to a mixture including an etchant and a controller". Accordingly Vahedi completely fails to disclose Applicants' recited "etching the material layer while protecting the photoresist layer from etching by exposing the integrated circuit device to a mixture including an etchant and a controller". Vahedi thus does not disclose each and every element that is recited in Claim 27, and therefore does not anticipate Claim 27 under §102. In other words, the Examiner has clearly failed to carry the burden of establishing a *prima facie* case of anticipation under §102.

Since the Examiner has failed to meet the minimum requirements needed to properly establish a case of anticipation under §102, it is respectfully submitted that the §102 rejection of Claim 27 lacks an essential element needed to properly establish a *prima facie* rejection, and therefore has a clear legal deficiency. Consequently, the rejection is clearly not proper and is without basis, and it is therefore respectfully requested that it be withdrawn.

#### Dependent Claim 28-31

Claims 28-31 depend from independent Claim 27. In the final rejection mailed on April 12, 2006, dependent Claims 28-31 were subject to the same rejection as independent Claim 27. In particular, Claims 28-31 were rejected under 35 U.S.C. §102 as anticipated by

Vahedi. However, Claims 28-31 are believed to be allowable over Vahedi, for example for the same reasons discussed above with respect to Claim 27, from which they depend.

Respectfully submitted,



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